BRIEF OF APPELLANT

1. Real Party In Interest.

   Applicant is the real party in interest.

2. Related appeals and interferences.

There are no related appeals or interferences directly affecting or that will be directly affected or that would have a bearing on the Board's decision in this appeal.

3. Status of claims.

Claims 1-24 were initially filed. Claims 1-24 were rejected a first time in an Office Action mailed on December 20, 2005. Claims 19, 20, 23 and 24 was amended a first time in Amendment A filed February 27, 2006. Claims 1-24 were finally rejected by a Final Office Action mailed March 15, 2006. Claims 1 and 9 were amended a first time, and claims 19 and 24 were amended a second time in Amendment AF filed on May 11, 2006. The amendments presented in Amendment AF were not entered as indicated in the Advisory Action mailed on May 26, 2006. Claims 1-24, including once amended claims 1, 9, 20 and 23 and twice amended claims 19 and 24 are pending and said claims 1-24 are appealed.

4. Status of amendments.

Amendment AF (the second amendment) was filed in the parent case on May 11, 2006 and was not entered, as indicated by the Advisory Action mailed May 26, 2006. No further amendments have been filed.

5. Summary of claimed subject matter.

The present invention generally relates to computer system buses and in particular, to a buffer bypass circuit for reducing latency in information transfers to a bus (Paragraph [0001]).

Regarding independent claim 1, the present invention provides a method for reducing latency in information transfers to a bus, comprising: receiving an indication that information is to be transferred to a bus; reading a bus grant indication; writing the information to a buffer if the bus grant indication does not indicate that transfer of the information to the bus is allowed; and transferring the information to the bus if the buffer is empty and the bus grant indication indicates that transfer of the information to the bus is allowed (Paragraph [0029]).

Regarding independent claim 9 of the present invention, and with reference to Fig. 5 and Paragraphs [0042] –[0044] the present invention provides a bus interface unit for reducing latency in information transfers from a device to a bus, comprising: a buffer **502** having inputs coupled to the device **104**; and logic **501** configured to receive an indication from the device **104** that information is to be transferred to the bus **106**, read a bus grant indication, and cause the information to either be stored in the buffer **502** if the bus grant indication does not indicate that transfer of the information from the device **104** to the bus **106** is allowed, or be transferred from the device **104** to the bus **106**, if the buffer **502** is empty and the bus grant indication indicates that transfer of the information to the bus **106** is allowed.

Regarding independent claim 19 of the present invention, and with reference to Fig. 5, and Paragraphs [0045] –[0046], the present invention provides a computer system including a bus with access governed by a bus arbiter employing a bus parking scheme and a buffer having inputs coupled to a device so that information to be transferred from the device to the bus is stored in the buffer if a grant indication generated by the bus arbiter indicates that the bus is unavailable for the transfer, a buffer bypass circuit for reducing latency in information transfers to the bus comprising: a multiplexer **503** having first inputs coupled to inputs to the buffer **502**, second inputs coupled to outputs of the buffer **502**, outputs coupled to the bus **106**, and at least one select input for selectively coupling either the first or the second inputs to the outputs; and logic **501** configured to provide control information to the at least one select input such that the first inputs are coupled to the outputs of the multiplexer **503** if the buffer **502** is empty and the bus grant indication indicates that the bus **106** is available for transfer of the information to the bus.

6. Grounds of rejection to be reviewed upon appeal.

Whether the Office erred in rejecting claims 1-24 under 35 U.S.C § 103(a) as being unpatentable over Applicants' Admitted Prior Art [hereinafter AAPA] in view of Park et al. (U.S. 5,526,508 A; hereinafter Park].

The claims on appeal stand or fall together; claims 1, 9 and 19 are independent claims.

7. Argument.

Refusal to enter amendment presented in Amendment AF

In the Advisory Action, mailed on May 25, 2005, the Office indicated that the proposed amendment filed after the final rejection, but prior to the date of filing a brief, would not be entered because they raise new issues that would require further consideration and/or search and they are not deemed to place the application in better form for appeal. More specifically, the Office states in the Advisory Action that the proposed amendment, "bypassing the buffer and transferring the information to the bus if the buffer is empty and the bus grant indication indicates that transfer of the information to the bus is allowed", in claim 1, raises a new issues which would not be considered, and which might extend the scope of the claimed invention. As such, the Office determined that the amendment would require further consideration and/or search, and would not be entered.

The amendment presented in the Amendment AF added the language, "bypassing the buffer and" to claim 1 as originally filed. While the Office has stated in the Advisory Action that the amendment would not be entered because it raises new issues, in the Final Office Action mailed on March 15, 2006, the Office stated that, "In other words, memory read data is directly transferred from main memory to CPU/Cache bus without using RD buffer (i.e. bypassing buffer) if said RD buffer is empty and said CPU/Cache bus is available to be used (viz., bus idle) for transferring read data into CPU/Cache (i.e. allowed)". As such, it appears that the Office had already interpreted the claim element as including "bypassing the buffer", before claim 1 was amended in the Amendment AF to specifically include the language. Accordingly, Applicants believe that the Office is incorrect in the determination that the amendment presented in response to the Final Office Action would require further consideration and/or search, and that the amendment should be entered for purposes of appeal. Accordingly, reversal of the refusal to enter the amendment presented in the Amendment AF is requested.

Claims 1-24 stand rejected under U.S.C. § 103(a) as being unpatentable over AAPA in view of Park et al.

In the Final Office Action, mailed on March 15, 2006, the Office rejected claims 1-24 under 35 U.S.C. § 103(e) as being unpatentable over AAPA in view of Park et al.

Claim 1 stands rejected under U.S.C. § 103(a) as being unpatentable over AAPA in view of Park et al.

Regarding independent claim 1, the Office states that the AAPA discloses a method for transferring information to a bus (i.e., Bus **106** of Fig. 1; See page 7, paragraph [0025], lines 1-3), comprising:

receiving an indication (i.e., CPU_WR_COM or CPU_RD_COM) that information (i.e., CAD, CDW, and CCO in Fig. 2-3) is to be transferred to a bus (i.e., Bus **106** of Fig. 1; See page 8, paragraph [0028]);

reading a bus grant indication (i.e., indication on GNT/PARKING-GNT in Fig. 2; See page 9, paragraph [0029]);

writing the information (i.e., said CAD, CDW, and CCO) to a buffer (i.e., Two-Entry Buffer **202** of Fig. 2) if the bus grant indication does not indicate that transfer of the information to the bus is allowed (i.e. when said GNT/PARKING-GNT is not active High, said Two-Entry Buffer is holding said information CAD, CDW, and CCO); and

transferring the information (i.e., said information CAD, CDW, and CCO in said Two-Entry Buffer) to the bus if the bus grant indication (i.e., said GNT/PARKING-GNT) indicates that transfer of the information to the bus is allowed (See page 9, paragraph [0029]).

Applicants respectfully disagree with the finding of the Office.

As stated in paragraph [0025] of the specification of the present invention as filed, "with the assistance of Control Logic **201**, the CPU **101** can write information to be transferred to the Bus **106** into the Buffer **201** regardless of whether the Bus **106** is busy or not, and the Control Logic **202** manages subsequent transfer of the written information from the Buffer **202** to the Bus **106** when the Bus **106** is available". As such, the AAPA describes transferring information through the Buffer **202**, regardless of whether or not a bus grant indication indicates that transfer of information to the Bus **106** is allowed. The Office incorrectly states that the AAPA teaches, "writing the information (i.e., said CAD, CDW, and CCO) to a buffer (i.e., Two-Entry Buffer **202** of Fig. 2) if the bus grant indication does not indicate that transfer of the information to the bus is allowed (i.e. when said GNT/PARKING-GNT is not active High, said Two-Entry Buffer is holding said information CAD, CDW, and CCO). This statement by the Office is incorrect because in the AAPA, the bus grant indication (i.e., GNT/PARKING-GNT) is not used to control the writing of information to the Buffer **202**, but rather is used to control the writing of

information to the Bus **106** from the Buffer **202**. The bus grant indication (i.e., GNT/PARKING-GNT) of the AAPA is described in paragraph [0029] as, "transfer of information from the Buffer **202** to the Bus **106** is initiated by the Control Logic **201** after receiving a grant indication on a grant line (GNT/PARKING-GNT)". As such, in the AAPA, the information is described as always being written to the Buffer **202**, then to the Bus **106**, regardless of the state of the bus grant indication (GNT/PARKING-GNT).

In summary, the Office incorrectly states that the AAPA teaches, "writing the information to a buffer if the bus grant indication does not indicate that transfer of the information to the bus is allowed", because in the AAPA writing of information to the buffer occurs regardless of whether or not the bus grant indication indicates that transfer of the information to the bus is allowed. In other words, in the AAPA, the bus grant indication does not control the writing of information to the buffer. As such, the Applicants conclude that the AAPA does not teach the claimed limitation of claim 1 of the present invention that includes, "writing the information to a buffer if the bus grant indication does not indicate that transfer of the information to the bus is allowed".

In the Final Office Action, the Office goes on to state that AAPA does not teach transferring the information to the bus if the buffer is empty and the transfer of the information to the bus is allowed, but that Park discloses a method for a cache line replacing system (See Fig. 3 and Abstract), wherein said method (i.e., said method for cache line replacing system) for reducing latency in information transfers (See col. 3, lines 2-3) to a bus (i.e., CPU/Cache bus 31 of Fig. 3) includes:

transferring information (i.e., line of cache data) to a bus (i.e., said CPU/Cache bus) if a buffer (i.e., RD buffer 36 of Fig. 3) is empty (i.e., said Buffer WT Reg counts 'zero'; See col. 5, lines 26-30) and transfer of the information to the bus is allowed (i.e., said CPU/Cache bus is idle after write-back data having been stored in write-back buffer; See col. 3, lines 27-35, and col. 4, lines 31-46).

The Office concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said method step of transferring, as disclosed by Park, in said method, as disclosed by AAPA, for the advantage of providing a way that a device (i.e., CPU) can read said information (i.e., data) at high speed without loss of said bus bandwidth (i.e., memory bus bandwidth; See Park, col. 6, lines 30-31).

The Office is combining the teaching of the AAPA and Park to arrive at the claimed element. The Office states that AAPA teaches part of the claim element, i.e., the bus grant indication indicates that transfer of the information to the bus is allowed, and that Park teaches the other part of the claim element, i.e., transferring the information to the bus if the buffer is empty and transfer of the information to the bus is allowed. As such, the Office relies on the combination of the buffer status as taught by Park with the bus grant indication as taught by the AAPA to arrive at the present invention.

Applicants respectfully disagree with the finding of the Office.

The Office contends that the claimed element step of, "the bus grant indication indicates that transfer of the information to the bus is allowed" is taught by AAPA at page 9, paragraph [0029]. However, what the AAPA states at paragraph [0029] is that, "transfer of information from the Buffer **202** to the Bus **106** is initiated by the Control Logic **201** after receiving a grant indication on a grant line (GNT/PARKING-GNT)". The Office has separated the claim elements of the claim such that the claim language is now being misinterpreted and the claim as a whole is not being considered. The elements of the claim which include, "writing the information to a buffer is the bus grant indication does not indicate that transfer of the information to the bus is allowed" and "transferring the information to the bus if the buffer is empty and the bus grant indication indicates that transfer of the information to the bus is allowed", make it very clear that that there are two scenarios, (1) if the bus grant indication indicates that transfer of the information to the bus is not allowed, then the information is written to the buffer, or (2) if the bus grant indication indicates that transfer of the information to the bus is allowed, and the buffer is empty, then the information is transferred to the bus. Interpreting the claim language as a whole makes it clear that the bus grant indication of the present invention controls the writing/transferring of information either (1) to the buffer or (2) directly to the bus, thereby bypassing the buffer. By contrast, AAPA teaches a GNT/PARKING-GNT signal that controls writing of information only from the buffer to the bus. There is no suggestion from the AAPA that the GNT/PARKING-GNT signal is used to control the transferring of information directly to the bus, thereby bypassing the buffer. As such, the GNT/PARKING-GNT signal as taught by the AAPA is not equivalent to the bus grant indication as described and claimed by the present invention. Accordingly, Applicants believe that the AAPA does not describe "the bus grant

indication indicates that transfer of the information to the bus is allowed", when the claim is taken as a whole.

In the Final Office Action and the Advisory Action, the Office states that Park discloses at col. 5, lines 16-35, that bypassing the RD buffer (i.e., buffer) and transferring the memory data (i.e., information) to the CPU/Cache Bus (i.e., bus) if the RD buffer (i.e., buffer) is empty after transferring CPU/Cache data 5 from said RD buffer during the cycle 402 in Fig. 4B and the reading address signal 42 of said CPU/Cache bus (i.e., signal for bus grant indication) indicates that transfer of the information to the CPU/Cache bus is allowed. As such, it appears that the Office has concluded that the "reading address signal 42 of said CPU/Cache bus is used to indicate that transfer of the information to the CPU/Cache bus is allowed", which is considered by the Office to be equivalent to the "bus grant indication indicates that transfer of the information to the bus is allowed" of the present invention.

Applicants disagree with this statement by the Office. Applicants contend that the read data is transmitted to the CPU/Cache bus with regard to the count value register, not with regard to the status of the CPU/Cache bus. As stated in Col. 5, lines 25-30, after all of the data stored in the read buffer has been read, that is the count value of the buffer count register becomes zero, the multiplexer switches over to connect the memory bus and data of the memory bus is transmitted directly to the CPU/Cache bus. The Park reference does not discuss the use of any type of bus grant request system to track the status of the CPU/Cache bus. As such, the Office's statement that Park discloses, "bypassing the RD buffer and transferring the memory data to the CPU/Cache Bus is the RD buffer is empty after transferring CPU/Cache data from said RD buffer and the reading address signal 42 of said CPU/Cache bus indicates that transfer of the information to the CPU/Cache bus is allowed" is incorrect.

At this time, Applicants would like to point out that there are inconsistencies in the examination of the claimed limitations that have made it difficult for the Applicant to respond to the Office Actions. More specifically, sometimes the Office states that Park does not describe the use of a grant indication, and that instead that element is described only by AAPA, such as in the statement in the second paragraph of the Advisory Action first continuation sheet, in which the Office States that, "Park teaches the step of bypassing the buffer and transferring the information to the bus if the buffer is empty and the transfer of the information to the bus is allowed". Whereas in the third paragraph of the same page, the Office states that "bypassing the

RD buffer (i.e., buffer) and transferring the memory data (i.e., information) to the CPU/Cache Bus (i.e., bus) if the RD buffer (i.e., buffer) is empty after transferring CPU/Cache data 5 from said RD buffer during the cycle 402 in Fig. 4B and the reading address signal 42 of said CPU/Cache bus (i.e., signal for bus grant indication) indicates that transfer of the information to the CPU/Cache bus is allowed". Accordingly, sometimes the Office states that the "bus grant indication" is taught only by the AAPA, and other times the Office appears to state that the "bus grant indication" is also described by Park. While the Office states several times throughout the Advisory Action that the Applicants have misinterpreted the claim rejection, the Applicants have merely attempted to respond to all the scenarios presented by the Office to formulate a complete and comprehensive response.

In the Final Office Action, the Office states that the AAPA does not teach the claimed subject matter, "transferring the information to the bus if the buffer is empty and the transfer of information to the bus is allowed", but that Park discloses a method for a cache line replacing system, wherein said method for reducing latency in information transfers to a bus includes transferring information (i.e., line of cache data) to a bus (i.e., said CPU/Cache bus) if a buffer (i.e., RD Buffer 36 of Fig. 3) is empty (i.e., said Buffer WT Reg counts 'zero'; See col. 5, lines 26-30) and transfer of the information to the bus is allowed (i.e., said CPU/Cache bus is idle after write-back data having been stored in write-back buffer; See col. 3, lines 27-35, and col. 4, lines 31-46). The Office reiterates in the Advisory Action, at paragraph four of continuation sheet 1, that "the primary reference AAPA teaches the claimed subject matter "bus grant indication", and the use of a bus grant request system to track the status of the bus, and that the secondary Park reference teaches the claimed subject matter "bypassing the buffer", therefore, the combination of AAPA and Park suggest the obviousness of the claimed invention. Accordingly, Applicants interpret the above statements by the Office to mean that the claimed subject matter, "transferring the information to the bus if the buffer is empty", is taught by the Park reference. However, the claimed subject matter of the present invention reads, "transferring the information to the bus if the buffer is empty **and** the bus grant indication indicates that transfer of the information to the bus is allowed". The Office has cited AAPA as teaching the use of a bus grant indication and so the Applicant will respond to the Office's statement that Park teaches, "transferring the information to the bus if the buffer is empty and transfer of the information to the bus is allowed."

Applicants contend that Park does not describe the claimed limitation of, "transferring the information to the bus if the buffer is empty and transfer of the information to the bus is allowed." The Office states that Park teaches transfer of the information to the bus is allowed (i.e., said CPU/Cache bus is idle after write-back data having been stored in write-back buffer; See col. 3, lines 27-35, and col. 4, lines 31-46). As such, the Office has concluded that the CPU/Cache bus being idle after write-back data having been stored in write-back buffer is equivalent to the claimed limitation that, "transfer of the information to the bus is allowed." Applicants disagree with this statement by the Office.

While the CPU/Cache bus as described by Park is idle after write-back data has been stored in the write-back buffer, this does not mean that transfer of information to the bus is allowed as claimed by the present invention. In order for the transfer of information to be "allowed" there must be something that is "allowing" the transfer. Simply because the CPU/Cache bus of Park is idle does not mean that transfer of said information to the bus is "allowed". Park does not describe a means for allowance or disallowance. The Office has additionally stated in the Final Office Action at Pg. 19, beginning at line 7, that Park discloses that the read data is transmitted with regard to the status of the CPU/Cache bus, thereby indicating that the CPU/Cache bus may be responsible for the transfer of the information to the bus being allowed. Applicants disagree with this statement by the Office. Applicants contend that the read data is transmitted to the CPU/Cache bus with regard to the count value register, not with regard to the status of the CPU/Cache bus. As stated in Col. 5, lines 25-30, after all of the data stored in the read buffer has been read, that is the count value of the buffer count register becomes zero, the multiplexer switches over to connect the memory bus and data of the memory bus is transmitted directly to the CPU/Cache bus. The Park reference does not discuss the use of any method or system that would indicate that transfer of the information to the bus is allowed. As such, Applicants contend that Park does not describe the claimed limitation of, "transferring the information to the bus if the buffer is empty and transfer of the information to the bus is allowed", as suggested by the Office.

At the bottom of Page 17 and the top of Page 18 of the Final Office Action, the Office summarizes its opinion by stating that Park clearly suggests the claimed limitation of, "transferring the information to the bus if the buffer is empty and the transfer of the information to the bus is allowed", and that while Park does not employ a bus grant indication or any other

form of indication as to whether or not the bus is available for transfer, that the AAPA teaches such a limitation. As such, the Office relies on the combination of the buffer status as taught by Park with the bus grant indication as taught by the AAPA to arrive at the invention.

Applicants believe that the Office's obviousness rejection is defective due to the inclusion of separate references to represent each of the different features described in the claims of the application. In fact, the Office has created features that do not exist in the claims by improper division of the claim language. With specific regard to claim 1, Applicants contend that the Office has lost sight of the claim as a whole and is attempting to piece together the claimed invention using the claims as a guide. The Office has taken the claim language of one of the claim limitations of claim 1 and separated it into pieces, then identified references that the Office believes teaches each of the pieces individually and then pieced the pieces back together to arrive at the claim language. More specifically, the Office has taken the claim element which states, "transferring the information to the bus if the buffer is empty and the bus grant indication indicates that transfer of the information to the bus is allowed", and separated it into two distinct elements, which include, "transferring the information to the bus if the bus grant indication indicates that transfer of the information to the bus is allowed", and "transferring the information to the bus if the buffer is empty". However, the claim as a whole does not provide these two distinct elements. In contrast, the claim language combines these two elements with a conjunctive "and" indicating that both conditions are required for the transfer of information. In other words, the claim language of claim 1 indicates that bypassing the buffer and transferring information to the bus occurs when the buffer is empty **and** the bus grant indication indicates that transfer of the information to the bus is allowed. Additionally, the Office has divided the claim element even more by breaking apart the element which states, "transferring the information to the bus if the bus grant indication indicates that transfer of the information to the bus is allowed", by addressing the use of a bus grant indication separately from the allowance of information transfer to the bus. By separating this statement, the Office has improperly interpreted the claim. The claim element depends upon the bus grant indication indicating that the transfer to the bus is allowed. Separating the bus grant indication from the element is improper and results in a misinterpretation of the claim language. In particular, the Office cites the Park reference to support bypassing the buffer and transferring information to the bus and the AAPA reference to support the use of a bus grant indication to indicate that the transfer of

information to the bus is allowed. However, the claim element states, "transferring the information to the bus **if** the bus grant indication indicates that transfer of the information to the bus is allowed". Clearly, the transfer of the information to the bus depends upon the bus grant indication as is evidenced by the use of the term "if" in the claim element. As such, it is improper to divide the claim element as presented by the Office and in so doing, the Office has lost sight of the claim as a whole.

Another issue before the Office is whether it would have been obvious to combine the references without having access to the application that is under examination to arrive at the claimed invention. In support of the combination of references, the Office states on Pg. 4 that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included the method step of transferring, as disclosed by Park, in said method, as disclosed by AAPA, the advantage of providing a way that a device (i.e. CPI) can read said information (i.e. data) at high speed without loss of said bus bandwidth (i.e. memory bus bandwidth; see Park, col. 6, lines 30-31). Applicants respectfully disagree with the determination by the Office regarding the combination of references.

Park teaches transferring information to the bus when the buffer is empty and the bus is "available", not that the transfer of the information to the bus is "allowed", which are two different things as explained above. The AAPA teaches the use of a bus grant indication to indicate that transfer of the information to the bus is "allowed". The Park reference does not provide any motivation to substitute the use of an indicator to indicate that transfer of the information to the bus is allowed. The Park reference does not address the need for any type of grant request indicators for the CPU/Cache bus. As such, the Applicants contend that the Office has improperly used the instant application as a basis for the motivation to combine or modify the prior art to arrive at the claimed invention.

To establish a *prima facie* case of obviousness, the prior art must cited must teach or suggest all the claim limitations. Neither the Park et al. reference nor the Applicants' Admitted Prior Art teach or suggest the step of transferring the information to the bus if the buffer is empty and the bus grant indication indicates that transfer of the information to the bus is allowed. Therefore, a *prima facie* case of obviousness has not been established because the cited references fail to disclose all the elements of the Applicants' invention.

Claim 9 stands rejected under U.S.C. § 103(a) as being unpatentable over AAPA in view of Park et al.

Regarding independent claim 9, the Office states in the Final Office Action that AAPA teaches logic configured to receive an indication (i.e., CPU_WR_COM or CPU_RD_COM) from the device (i.e., said CPU) that information (i.e., CAD, CDW, and CCO in Fig. 2-3) is to be transferred to the bus (i.e., said Bus; See page 8, paragraph [0028]), read a bus grant indication (i.e., indication on GNT/PARKING-GNT in Fig. 2; See page 9, paragraph [0029]), and cause the information (i.e., said CAD, CDW, and CCO) to either be stored in the buffer (i.e., said Two-Entry Buffer) if the bus grant indication does not indicate that transfer of the information from the device (i.e., said CPU) to the bus is allowed (i.e., when said GNT/PARKING-GNT is not active High, said Two-Entry Buffer is holding said information CAD, CDW and CCO), or be transferred from the buffer (i.e., said Two-Entry Buffer) to the bus if the bus grant indication (i.e., said GNT/PARKING-GNT) indicates that transfer of the information from the buffer to the bus is allowed (See page 9, paragraph [0029]). As such, the Office contents that the GNT/PARKING-GNT of the AAPA is equivalent to the bus grant indication of the present invention that causes the information to either be stored in the buffer if the bus grant indication does not indicate that transfer of the information from the device to the bus is allowed, or be transferred from the buffer to the bus if the bus grant indication indicates that transfer of the information from the buffer to the bus is allowed.

Applicants disagree with this finding by the Office. The statement by the Office that the GNT/PARKING-GNT signal is an indicator that causes the information to be stored in the buffer if the GNT/PARKING-GNT does not indicate that transfer of the information from the device to the bus is allowed is incorrect. The GNT/PARKING-GNT as described by AAPA does not control whether the information is written to the buffer. In the AAPA, the information is always written to the buffer and the GNT/PARKING-GNT is used to indicate that the information can be transferred from the buffer to the bus. As such, the AAPA does not described the claimed limitation as suggested by the Office.

Additionally, the Office states AAPA does not teach logic being configured to cause the information to be transferred from the device to the bus if the buffer is empty and the transfer of the information to the bus is allowed, but that Park does discloses logic configured to cause information to be transferred from the device to the bus if the buffer is empty and transfer of the

information to the bus is allowed. The Office cites the MUX **38** and Buffer WT Reg **37** of Fig. 3 in support of this statement. Additionally, the Office states that the CPU/Cache bus is idle after the write-back data is stored in the write-back buffer and as such, the transfer of the information to the bus is allowed.

Applicants respectfully disagree with the finding of the Office. As detailed with regard to independent claim 1, just because the CPU/Cache bus is idle after write-back data has been stored in the write-back buffer, does not mean that transfer of information to the bus is allowed, as claimed by the present invention. The claim must be considered as a whole and in doing so it is clear that the bus grant indication is the means through which the system of the present invention indicates that the transfer of information to the bus is allowed. The bus grant indication in accordance with the present invention indicates that the specific information which is requesting transfer to the bus has been allowed access to the bus. It is not simply that the bus is idle, but that an indication has been made by a bus grant indication that specific information is allowed to be transferred to the bus. This "allowance of transfer" is not equivalent to the bus being idle and "available for transfer". For the reasons cited above, Applicants contend that Park does not describe logic configured to cause information to be transferred from the device to the bus if the buffer is empty and transfer of the information to the bus is allowed.

The Office concludes with regard to independent claim 9 that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said logic, as disclosed by Park, in said logic as disclosed by AAPA, for the advantage of providing a way that said device can read information at high speed without loss of said bus bandwidth.

The Applicants respectfully disagree with the Office's conclusion regarding the motivation to combine the references as suggested by the Office. As previously detailed with regard to independent claim 1, Applicants contend that the Park reference does not provide any motivation to substitute the use of a bus grant indication to indicate that transfer of the information to the bus is allowed. The Park reference does not address the need for any type of grant request indicators for the CPU/Cache bus. As such, the Applicants contend that the Office has improperly used the instant application as a basis for the motivation to combine or modify the prior art to arrive at the claimed invention.

Claim 19 stands rejected under U.S.C. § 103(a) as being unpatentable over AAPA in view of Park et al.

Regarding independent claim 19, the Office states that AAPA does not teach a buffer bypass circuit for reducing latency in information transfers to the bus comprising: a multiplexer having first inputs coupled to the inputs of the buffer, second inputs coupled to outputs of the buffer, outputs coupled to the bus, and at least one select input for selectively coupling either the first or the second inputs to the outputs; and logic configured to provide control information to the at least one select input such that the first inputs are coupled to the outputs of the multiplexer if the buffer is empty and the bus is available for transfer of the information to the bus. However, the Office goes on to state that Park discloses a cache line replacement apparatus, wherein a buffer bypass circuit for reducing latency in information transfers to a bus comprising: a multiplexer having first inputs coupled to inputs to a buffer; second inputs coupled to the outputs of the buffer; outputs coupled to the bus; at least one select input for selectively coupling either the first or the second inputs to the outputs; and logic configured to provide control information to the at least one select input such that the first inputs are coupled to the outputs of the multiplexer if the buffer is empty and the bus is available for transfer of the information to the bus.

Applicants respectfully disagree with the conclusion of the Office. Claim 19 of the present invention includes, "at least one select input for selectively coupling either the first or the second inputs to the outputs; and logic configured to provide control information to the at least one select input such that the first inputs are coupled to the outputs of the multiplexer if the buffer is empty and the bus is available for transfer of the information to the bus." As such, the control information couples the first inputs of the multiplexer to the outputs of the multiplexer, which are coupled to the bus, if the buffer is empty and the bus is available for transfer of the information to the bus. The Office states that Park teaches that the bus is available for transfer of the information to the bus, as supported by col. 3, lines 27-35, and col. 4, lines 31-46, in which the CPU//Cache bus is idle after write-back data having been stored in write-back buffer. As detailed with regard to independent claim 1, just because the CPU/Cache bus is idle after write-back data has been stored in the write-back buffer, does not mean that the bus is available for transfer of "the" information to the bus, as claimed by the present invention. The availability of the bus is determined by the grant indication of the present invention. The claim must be considered as a whole and in doing so it is clear that the bus grant indication is the means through which the system of the present invention indicates that the bus is available for transfer

of the information to the bus. It is not simply that the bus is idle, but that an indication has been made by a bus grant indication that the bus is available for the transfer of identified information to the bus. For the reasons cited above, Applicants contend that Park does not describe logic configured to provide control information to the at least one select input such that the first inputs are coupled to the outputs of the multiplexer if the buffer is empty and the bus is available for transfer of the information to the bus.

The Office concludes that it would have been obvious to one of ordinary skill in the art at the time the invention was made to have included said buffer bypass circuit, as disclosed by Park in said logic, as disclosed by AAPA, for the advantage of providing a way that said device can read said information at high speed without loss of said bus bandwidth.

The Applicants respectfully disagree with the Office's conclusion regarding the motivation to combine the references as suggested by the Office. As previously detailed with regard to independent claim 1, Applicants contend that the Park reference does not provide any motivation to substitute the use of a bus grant indication to indicate that the bus is available for transfer of the information to the bus. The Park reference does not address the need for any type of grant request indicators for the CPU/Cache bus. As such, the Applicants contend that the Office has improperly used the instant application as a basis for the motivation to combine or modify the prior art to arrive at the claimed invention.

For the reasons cited above, Applicant believes that independent claims 1, 9 and 19 are patentable over Applicants' Admitted Prior art in view of Park et al. and that Applicant's patent rights have clearly been unfairly denied.

The Office's unfair refusal to consider this significant distinction between the claimed invention and the clear teachings and suggestions of the prior art has lead to an unfair denial of Applicant's patent rights.

Accordingly, reversal of the final rejection is solicited. No fair interpretation of the prior art can support the Office's position.

8. Claims Appendix.

1. (Previously Amended) A method for reducing latency in information transfers to a bus, comprising:

receiving an indication that information is to be transferred to a bus;

reading a bus grant indication;

writing the information to a buffer if the bus grant indication does not indicate that transfer of the information to the bus is allowed; and

transferring the information to the bus if the buffer is empty and the bus grant indication indicates that transfer of the information to the bus is allowed.

2. (Original) The method according to claim 1, wherein the information includes a write command, an address, and data to be written to the address.

3. (Original) The method according to claim 2, wherein the indication that information is to be transferred to the bus includes the write command.

4. (Original) The method according to claim 1, wherein the information includes a read command and an address from which data is to be read.

5. (Original) The method according to claim 4, wherein the indication that information is to be transferred to the bus includes the read command.

6. (Original) The method according to claim 1, wherein access to the bus is controlled by a bus arbiter employing a bus parking protocol.

7. (Original) The method according to claim 6, further comprising sending a bus access request to the bus arbiter if the bus grant indication does not indicate that transfer of the information to the bus is allowed.

8. (Original) The method according to claim 7, further comprising periodically sending bus access requests to the bus arbiter and reading the bus grant indication if the information stored in

the buffer has not been transferred to the bus, so that when the bus grant indication indicates that transfer of the information to the bus is allowed, the information stored in the buffer is transferred to the bus.

9. (Previously Amended) A bus interface unit for reducing latency in information transfers from a device to a bus, comprising:

a buffer having inputs coupled to the device; and

logic configured to receive an indication from the device that information is to be transferred to the bus, read a bus grant indication, and cause the information to either be stored in the buffer if the bus grant information does not indicate that transfer of the information from the device to the bus is allowed, or be transferred from the device to the bus if the buffer is empty and the bus grant indication indicates that transfer of the information to the bus is allowed.

10. (Original) The bus interface unit according to claim 9, wherein the information includes a write command, an address, and data to be written to the address.

11. (Original) The bus interface unit according to claim 10, wherein the indication from the device that information is to be transferred to the bus includes the write command.

12. (Original) The bus interface unit according to claim 9, wherein the information includes a read command and an address from which data is to be read.

13. (Original) The bus interface unit according to claim 12, wherein the indication from the device that information is to be transferred to the bus includes the read command.

14. (Original) The bus interface unit according to claim 9, wherein access to the bus is controlled by a bus arbiter employing a bus parking protocol.

15. (Original) The bus interface unit according to claim 14, wherein the logic is further configured to send a bus access request to the bus arbiter if the bus grant indication does not indicate that transfer of the information to the bus is allowed.

16. (Original) The bus interface unit according to claim 15 wherein the logic is further configured to periodically send bus access requests to the bus arbiter and read the bus grant indication if the information stored in the buffer has not been transferred to the bus, so that when the bus grant indication indicates that transfer of the information to the bus is allowed, the logic causes the information stored in the buffer to be transferred to the bus.

17. (Original) The bus interface unit according to claim 9, wherein the logic includes a multiplexer having first inputs coupled to the buffer inputs, second inputs coupled to the buffer outputs, outputs coupled to the bus, and at least one select input for selectively coupling either the first or the second inputs to the outputs; and the logic is further configured to provide a control output to the at least one select input so that the first inputs are coupled to the outputs if the bus grant indication indicates that transfer of the information to the bus is allowed and the buffer is empty.

18. (Original) The bus interface unit according to claim 17, wherein the logic is further configured to provide the control output to the at least one select input so that the second inputs are coupled to the outputs if the bus grant indication does not indicate that transfer of the information to the bus is allowed.

19. (Previously Amended) In a computer system including a bus with access governed by a bus arbiter employing a bus parking scheme and a buffer having inputs coupled to a device so that information to be transferred from the device to the bus is stored in the buffer if a grant indication generated by the bus arbiter indicates that the bus is unavailable for the transfer, a buffer bypass circuit for reducing latency in information transfers to the bus comprising:

a multiplexer having first inputs coupled to inputs to the buffer, second inputs coupled to outputs of the buffer, outputs coupled to the bus, and at least one select input for selectively coupling either the first or the second inputs to the outputs; and

logic configured to provide control information to the at least one select input such that the first inputs are coupled to the outputs of the multiplexer if the buffer is empty and the bus grant indication indicates that the bus is available for transfer of the information to the bus.

20. (Previously Amended) The buffer bypass circuit claimed in claim 19, wherein the logic is further configured to provide control information to the at least one select input generated such that after checking the bus grant indication the second inputs are coupled to the outputs of the multiplexer if the buffer is not empty and the bus grant indication indicates that the bus is available for transfer of the information to the bus, or the bus grant indication does not indicate that the bus is available for transfer of the information to the bus.

21. (Original) The buffer bypass circuit according to claim 19, wherein the information includes a write command, an address, and data to be written to the address.

22. (Original) The buffer bypass circuit according to claim 19, wherein the information includes a read command and an address from which data is to be read.

23. (Previously Amended) The buffer bypass circuit according to claim 19, wherein the logic is further configured to send a bus access request to the bus arbiter if the bus grant indication does not indicate that the bus is available for transfer of the information to the bus.

24. (Previously Amended) The buffer bypass circuit according to claim 23, wherein the logic is further configured to periodically send bus access requests to the bus arbiter and read the ensuing bus grants if the information stored in the buffer has not been transferred to the bus, so that when one of the ensuing bus grants indications indicates that the bus is available for transfer of the information to the bus, the information stored in the buffer is transferred to the bus.

9. Evidence Appendix.

None

10. Related Proceedings Appendix.

None